What is claimed is:

1. A thin film transistor comprising:

a lamination layer comprising a first conductive film, a first insulating film, and a second conductive film, which is sequentially laminated over an insulating surface;

a semiconductor film formed in contact with a side surface of the lamination layer; and

a third conductive film covering the semiconductor film with a second insulating film interposed therebetween,

wherein a channel forming region is formed in a region of the semiconductor film contacting with the first insulating film and the third conductive film, and

wherein the third conductive film is a gate electrode.

2. A thin film transistor according to claim 1, wherein the first conductive film and the second conductive film are a source electrode or a drain electrode,

3. A thin film transistor according to claim 1, wherein the third conductive film covers at least the semiconductor film contacting with the first insulating film, with the second insulating film interposed therebetween.

4. A thin film transistor according to claim 1, the third conductive film covers a part of the semiconductor film contacting with the first insulating film, with the second insulating film interposed therebetween.

5. A thin film transistor according to claim 1, wherein the channel forming region of the semiconductor film has a closed contour shape.

6. A thin film transistor according to claim 1, wherein a side surface of the lamination layer is slanted to the insulating surface.

7. A thin film transistor according to claim 1, wherein the source electrode or the drain electrode has a different film thickness in a central part thereof and a edge portion thereof.

8. A thin film transistor comprising:

a lamination layer comprising n conductive films and (n-1) insulating films, which are alternately laminated over an insulating surface;

a semiconductor film formed in contact with a side surface of the lamination layer; and

a second conductive film covering the semiconductor film with a second insulating film interposed therebetween,

wherein n is an integer of 2or more,

wherein, among the n conductive films, a conductive film contacting with the insulating surface and a conductive film which is farthest from the conductive film contacting with the insulating surface are a source electrode and a drain electrode, respectively,

wherein a channel forming region is formed in a region of the semiconductor film contacting with the (n-1) insulating films and the third conductive film, and

wherein the second conductive film is a gate electrode.

9. A thin film transistor according to claim 8, wherein the second conductive film covers at least the semiconductor film contacting with the (n-1) insulating films, with the second insulating film interposed therebetween.

10. A thin film transistor according to claim 8, the second conductive film covers a part of the semiconductor film contacting with the (n-1) insulating films, with the second insulating film interposed therebetween.

11. A thin film transistor according to claim 8, wherein the channel forming

region of the semiconductor film has a closed contour shape.

12. A thin film transistor according to claim 8, wherein a side surface of the lamination layer is slanted to the insulating surface.

13. A thin film transistor according to claim 8, wherein the source electrode or the drain electrode has a different film thickness in a central part thereof and a edge portion thereof.

14. A method for manufacturing a thin film transistor comprising:

forming a lamination layer by laminating a first conductive film, a first insulating film, a second conductive film over an insulating surface in sequence;

etching the laminating layer; and

laminating a semiconductor film, a second insulating film, and a third conductive film over a side surface of the lamination layer in sequence so as to form a gate insulating film and a gate electrode.

15. A method according to claim 14, wherein etching is performed so that the side surface of the lamination layer is slanted to the insulating surface.

16. A method for manufacturing a thin film transistor comprising:

forming a first conductive film over an insulating surface;

etching the first conductive film into a desired shape so as to form a first electrode;

forming a first insulating film over the first electrode and the insulating surface;

forming a second conductive film over the first insulating film;

exposing a side surface of the first electrode, the first insulating film, and the second electrode by etching the second conductive film and the first insulating film into a desired shape so as to form a second electrode;

forming a semiconductor film over the exposed side surface;

etching the semiconductor film into a desired shape;

forming a second insulating film and a third conductive film over the semiconductor film in sequence;

etching the third conductive film into a desired shape so as to form a gate electrode.

17. A method according to claim 16, wherein the exposed side surface is etched so as to be slanted to the insulating surface.

18. A method for manufacturing a thin film transistor comprising:

forming a first conductive film over an insulating surface;

etching the first conductive film so as to form a first electrode;

forming a first insulating film over the first electrode and the insulating surface,;

etching the first insulating film so as to expose a part of the first electrode;

forming a second conductive film over the first insulating film and the first electrode;

etching the second conductive film so as to expose a part of the first electrode and a part the first insulating film, and forming a second electrode;

forming a semiconductor film over the exposed surface of the first electrode, the exposed surface of the first insulating film, and the a part of the second electrode;

etching the semiconductor film into a desired shape;

forming a second insulating film and a third conductive film over the semiconductor film in sequence; and

etching the third conductive film into a desired shape so as to form a gate electrode.

19. A method according to claim 18, wherein the exposed surface is etched so as to be slanted to the insulating surface.